Notice of References Cited	Application/Control No. 09/955,993	Applicant(s)/Patent Under Reexamination TOYONOH ET AL.	
	Examiner Chat C. Do	Art Unit 2124	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,065,032	05-2000	Nicol, Christopher John	708/628
*	B	US-5,151,875	09-1992	Sato, Tai	708/626
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Kiwon et al., Design of a high performance 32x32 bit multiplier with a novel sign select Booth encoder, 2001, IEEE, pages 701-704.
	V	Issam et al., Circuit techniques for CMOS low-power high-performance multipliers, 1996, IEEE Journal of solid-state circuits, Vol. 31, No. 10, pages 1535-1546.
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.